WHAT IS CLAIMED IS:

1. A source synchronous receiver comprising:

a data buffer configured to receive data through one or more signal lines;

a clock receiver comprising a clock signal buffer and a clock detector, wherein the clock signal buffer is configured to receive a first clock signal and drive a second clock signal responsive to receiving the first clock signal, and wherein the clock detector is configured to assert a clock detect signal responsive to receiving the first clock signal;

a digital locked loop (DLL) circuit configured to receive the second clock signal from the clock buffer, wherein the DLL circuit is configured to drive the second clock signal to the data buffer;

a clock verification circuit, wherein the clock verification circuit is configured to receive the clock detect signal from the clock detector, and wherein the clock verification circuit is configured to reset the source synchronous receiver responsive to a failure to receive clock detect signal.

2. The source synchronous receiver as recited in claim 1, wherein the DLL circuit is configured to assert a lock detect signal, and wherein the clock verification circuit is further configured to reset the source synchronous receiver responsive to a failure of the clock verification circuit to receive the lock detect signal.

3. The source synchronous receiver as recited in claim 2, wherein the clock verification circuit is configured to assert a DLL lock signal responsive to receiving both the clock detect signal and the lock detect signal, and wherein the clock verification circuit is configured to reset the source synchronous receiver by de-asserting the DLL lock signal.

4. The source synchronous receiver as recited in claim 2, wherein resetting the source synchronous receiver includes powering down the clock signal buffer responsive to a failure of the clock detector failing to detect the first clock signal.

5. The source synchronous receiver as recited in claim 4, wherein the clock signal buffer is powered on responsive to the clock detector detecting the first clock signal.

6. The source synchronous receiver as recited in claim 2, wherein the source synchronous receiver is coupled to the core logic of an integrated circuit, wherein the core logic is configured to receive data from the data buffer.

7. The source synchronous receiver as recited in claim 6, wherein the clock verification circuit is configured to drive the DLL lock signal to a status register in the core logic.

8. The source synchronous receiver as recited in claim 1, wherein the first clock signal is a differential clock signal and the second clock signal is a single-ended clock signal.

9. The source synchronous receiver as recited in claim 2, wherein the clock verification circuit includes a chain of serially coupled flip-flops, wherein the chain includes at least two flip-flops.

10. The source synchronous receiver as recited in claim 9, wherein the clock verification circuit is configured to receive a third clock signal, wherein each of the flip-flops receives the third clock signal.

11. The source synchronous receiver as recited in claim 10, wherein the DLL lock signal is not asserted until at least two cycles of the third clock signal have completed.

12. The source synchronous receiver as recited in claim 1, wherein the source synchronous receiver is configured to be hot swappable.

13. The source synchronous receiver as recited in claim 1, wherein the clock verification circuit is further configured to assert a receiver enable signal.

14. The source synchronous receiver as recited in claim 13, wherein the clock verification circuit is further configured to receive a test mode signal, and wherein the receiver enable signal is de-asserted responsive to the clock verification responsive to receiving the test mode signal, and wherein the clock verification circuit is inhibited from resetting the source synchronous receiver responsive to receiving the test mode signal.

15. The source synchronous receiver as recited in claim 1, wherein the clock verification circuit is further configured to receive a reset mask signal, wherein the clock verification circuit is configured to inhibit a reset of the source synchronous receiver responsive to receiving the reset mask signal.

16. The source synchronous receiver as recited in claim 1, wherein the DLL circuit and the clock verification circuit are powered down responsive to a failure of the clock detect circuit to detect the first clock signal.

17. The source synchronous receiver as recited in claim 1, wherein the clock verification circuit is configured to perform a local reset of the source synchronous receiver.

18. A method for operating a source synchronous receiver, the method comprising

detecting a first clock signal with a clock detector;

producing a second clock signal responsive to a clock signal buffer receiving the first clock signal, and regenerating the second clock signal using a digital locked loop (DLL) circuit;

receiving a clock detect signal from the clock detector, said receiving performed by a clock verification circuit;

resetting the source synchronous receiver responsive to a failure of the clock verification circuit to receive the clock detect signal.

19. The method as recited in claim 18 wherein the DLL circuit is configured to assert a lock detect signal, and wherein the clock verification circuit is further configured to reset the source synchronous receiver responsive to a failure of the clock verification circuit to receive the lock detect signal.

20. The method as recited in claim 19, wherein the clock verification circuit is further configured to assert a DLL lock signal.

21. The method as recited in claim 20 further comprising de-asserting the DLL lock signal responsive to a failure of the clock verification circuit to receive the clock detect signal or the lock detect signal, wherein said de-asserting the DLL lock signal causes the resetting of the source synchronous receiver.

22. The method as recited in claim 20 further comprising the clock verification circuit driving the DLL lock signal to a status register, wherein the status register is located in core logic of an integrated circuit, and wherein the source synchronous receiver is coupled to the core logic.

23. The method as recited in claim 22 further comprising delaying said driving of the DLL lock signal by two or more clock cycles of a third clock signal, wherein the clock verification circuit includes a chain of serially coupled flip-flops including at least two flip-flops, and wherein each of the flip-flops is configured to receive the third clock signal.

24. The method as recited in claim 18 further comprising powering down the clock signal buffer responsive to the clock detector failing to detect the first clock signal.

25. The method as recited in claim 24 further comprising powering on the clock signal buffer responsive to the clock detector detecting the first clock signal.

26. The method as recited in claim 18 further comprising the DLL circuit driving the second clock signal to a data buffer, wherein the data buffer is configured to receive data through one or more data lines.

27. The method as recited in claim 18, wherein the first clock signal is a differential signal and the second clock signal is a single-ended signal.

28. The method as recited in claim 18 further comprising the clock verification circuit asserting a receiver enable signal.

29. The method as recited in claim 28, wherein the clock verification circuit is configured de-assert the receiver enable signal responsive to receiving a test mode signal.

30. The method as recited in claim 29 further comprising inhibiting the clock verification circuit from resetting the source synchronous receiver responsive to said receiving a test mode signal.

31. The method as recited in claim 18 further comprising inhibiting the clock verification circuit from resetting the source synchronous receiver responsive to receiving a reset mask signal.

32. The method as recited in claim 18 further comprising powering down the DLL circuit and the clock verification circuit responsive to a failure of the clock detector to detect the first clock signal.

33. The method as recited in claim 32 further comprising powering on the DLL circuit and the clock verification circuit responsive to the clock detector detecting the first clock signal.

34. The method as recited in claim 18, wherein said resetting the source synchronous receiver is performed locally.